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TITLE OF THE INVENTION

FREQUENCY SELECTION OF SWITCH MODE POWER CONVERTERS VIA SOFTSTART VOLTAGE LEVEL

10 CROSS REFERENCE TO RELATED APPLICATIONS

N/A

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

15 N/A

BACKGROUND OF THE INVENTION

The present application relates generally to switch mode power supplies, and more specifically to switch mode 20 power converters providing improved control of in-rush current and output voltage overshoot.

In recent years, the need for switch mode power supplies or DC-to-DC converters has risen dramatically as Integrated Circuits (ICs) such as Digital Signal 25 Processors (DSPs) and mixed signal ICs have continued to decrease in size while their power consumption has increased. Switch mode power converters are typically employed in such ICs for converting positive or negative input supply voltages to output supply voltage levels 30 that are appropriate for powering circuitry within the IC

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and/or for powering circuitry externally connected to the IC. For example, a switch mode power converter may be configured for either increasing or decreasing an input supply voltage level provided to an IC.

5   Conventional switch mode power converters typically include at least one soft-start circuit configured to limit in-rush currents at start-up. For example, an excessive in-rush current can cause an output voltage overshoot, which can disrupt the operation of a system

10   processor by triggering unwanted resets. Further, excessive in-rush currents can increase the maximum current through converter components and require the use of components with increased maximum current ratings, significantly increasing the overall cost of the

15   converter. A soft-start circuit typically feeds a constant current to an external capacitor to charge the capacitor, thereby ramping supply and reference voltages within the converter and limiting in-rush currents.

          One drawback of conventional switch mode power

20   converters is that the soft-start circuits employed therewith often do not successfully limit in-rush currents for all power converter frequencies. For example, a soft-start circuit may sufficiently limit in-rush currents when the converter operates at relatively

25   low frequencies, but the soft-start circuit may be unable to limit in-rush currents at higher converter frequencies. As a result, while output voltage overshoots caused by excessive in-rush currents may be effectively eliminated at high duty ratios and low

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frequencies, output voltage overshoots may persist at low duty ratios and high frequencies.

Moreover, conventional switch mode power converters typically require more than one input for programming the soft-start timing and the converter frequency selection, thereby increasing the number of pins on the IC package and increasing costs.

It would therefore be desirable to have a switch mode power converter that limits the in-rush current at start-up over a range of switching frequencies and avoids the drawbacks of the above-described conventional switch mode power converters.

BRIEF SUMMARY OF THE INVENTION

In accordance with the present invention, a switch mode power converter is provided that limits the in-rush current at start-up and reduces the occurrence of output voltage overshoot over a substantial range of switching frequencies. Benefits of the presently disclosed switch mode power converter are achieved by linking soft-start programming to the selected switching frequency of the converter.

In one embodiment, the switch mode power converter includes at least one Soft-Start(SS)/Frequency-Select(FS) input, at least one oscillator enable input, and an oscillator having at least one control input. The oscillator is operative to generate a selected one of a plurality of frequencies based on the state of the control input. The SS/FS input is connectable to ground

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(1) via an external capacitor, or (2) via the external capacitor and an external resistor connected in parallel. In the event only the external capacitor is connected between the SS/FS input and ground, an open circuit is

5   effectively formed between the SS/FS input and ground for Direct-Current (DC). In the event the parallel combination of the external capacitor and the external resistor is connected between the SS/FS input and ground, a resistive path is made available from the SS/FS input

10 to ground. In effect, the SS/FS input has a high logical state when only the external capacitor is connected between the SS/FS input and ground, and the SS/FS input has a low logical state when the external capacitor and the external resistor are connected in parallel between

15 the SS/FS input and ground. At least one control signal representative of the state of the SS/FS input is applied to the oscillator control input, which is employed to select the frequency generated by the oscillator.

In the presently disclosed switch mode power

20 converter, soft-start programming is linked to the frequency selection of the converter. The soft-start programming is accomplished via one or more external capacitive and/or resistive components connected between the SS/FS input and ground. In the presently disclosed

25 embodiment, an external capacitor having a predetermined value connected between the SS/FS input and ground is employed to program the soft-start time based on the value of the capacitor. A constant current fed to the external capacitor ramps the voltage level at the SS/FS

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input during start-up. The switching frequency generated by the oscillator is selected via the state of the SS/FS input. In the preferred embodiment, the switch mode power converter includes dual SS/FS inputs. The oscillator generates (1) a high switching frequency when only external capacitors are connected between the respective SS/FS inputs and ground, (2) a low switching frequency when parallel combinations of an external capacitor and an external resistor are connected between the respective SS/FS inputs and ground, and (3) an intermediate switching frequency when only an external capacitor is connected between one of the SS/FS inputs and ground, and a parallel combination of an external capacitor and an external resistor is connected between the other SS/FS input and ground.

By providing a switch mode power converter in which soft-start programming is linked to the frequency selection of the converter, in-rush current at start-up and output voltage overshoot can be decreased over a range of switching frequencies. Further, because the switching frequency is determined by the state of the SS/FS input, both the soft-start timing and the switching frequency selection can be programmed via the same input pin, thereby obviating the need for separate pins to program the soft-start timing and the switching frequency of the converter.

Other features, functions, and aspects of the invention will be evident from the Detailed Description of the Invention that follows.

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BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The invention will be more fully understood with reference to the following Detailed Description of the Invention in conjunction with the drawings of which:

Fig. 1 is a schematic diagram of a typical application of a switch mode power converter according to the present invention;

Fig. 2 is a schematic diagram of soft-start circuitry within the switch mode power converter of Fig. 1 for limiting the in-rush current at start-up and reducing output voltage overshoot; and

Figs. 3a-3b are timing diagrams illustrating soft-start signals generated by the soft-start circuitry of Fig. 2.

DETAILED DESCRIPTION OF THE INVENTION

A switch mode power converter is disclosed that is capable of limiting the in-rush current at start-up and reducing the occurrence of output voltage overshoot over a range of converter frequencies. The presently disclosed switch mode power converter includes soft-start circuitry in which soft-start programming is linked to the frequency selection of the converter.

Fig. 1 depicts an illustrative embodiment of an application of a Switch Mode Power Converter (SMPC) 100, in accordance with the present invention. As shown in Fig. 1, the SMPC 100 includes Soft-Start/Frequency-Select (SS/FS) inputs 1-2, inputs INV1-INV2 and outputs $EAMP_{OUT1}$-

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EAMP$_{OUT2}$ corresponding to respective error amplifiers 1-2 within the SMPC 100, and inputs ENBL1-ENBL2 for enabling the operation of the SMPC 100. It is noted that details of the structure and operation of the illustrative switch mode power converter 100 of Fig. 1 are described in the data sheet Dual, Voltage Mode, DDR Selectable, Synchronous, Step-Down Controller for Notebook System Power, TPS51020, Texas Instruments® Incorporated, SLUS564A – July 2003 – revised November 2003, pages 1-24, which is incorporated herein by reference.

Fig. 2 depicts an illustrative embodiment of Switch Mode Power Converter (SMPC) circuitry 200 included in the SMPC 100 of Fig. 1. In the illustrated embodiment, the SMPC circuitry 200 includes dual soft-start circuits (SSCKTs) 1-2, the plurality of error amplifiers (EAMPs) 1-2, a plurality of comparators (COMPs) 1-2, an oscillator 202 including oscillator control logic circuitry 204, and enable logic circuitry 1-2 for enabling the operation of the oscillator 202. The soft-start circuits 1-2 include the respective Soft-Start/Frequency-Select (SS/FS) inputs 1-2, respective resistors R$_s$1-R$_s$2, respective current sources I$_s$1-I$_s$2, and respective NMOS Field Effect Transistors (FETs) M1-M2. The SMPC circuitry 200 further includes voltage references VREF1A-VREF2A coupled to non-inverting inputs of the error amplifiers 1-2, respectively. Moreover, the comparators 1-2 have suitable voltage reference values VREF1B-VREF2B connected to their respective inverting inputs. The comparators 1-2 provide frequency select

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(FREQSEL) signals 1-2 to the oscillator 202, which is operative to generate an oscillator output signal (OSC_{OUT}) having a frequency that is selected based on the states of the signals FREQSEL1-FREQSEL2.

5   It is appreciated that the switch mode power converter circuitry 200 comprises a portion of the switch mode power converter 100 (see Fig. 1), such as the above-mentioned TPS51020 switch mode power converter manufactured by Texas Instruments® Incorporated or any

10   other suitable switch mode power converter device. Specifically, the SMPC circuitry 200 comprises the portion of the switch mode power converter 100 that relates to soft-start programming and switching frequency selection. It should be noted, however, that the SMPC

15   circuitry 200 including the soft-start circuits 1-2 (SSCKT1-SSCKT2) may be employed in any other suitable circuit application.

In the preferred embodiment, each of the error amplifiers 1-2 has a wide-bandwidth and a low output

20   impedance, and is employed as a voltage servo control block in a Pulse Width Modulation (PWM) control block utilizing a fixed-frequency, feed-forward, voltage-mode control scheme. For example, in the event the error amplifiers 1-2 are employed in conjunction with the

25   above-mentioned TPS51020 SMPC device, such a control scheme provides efficient down conversion with good line regulation and fast transient response. Further, loop compensation may be programmed by connecting external filter networks between the outputs $EAMP_{OUT1}$-$EAMP_{OUT2}$ and

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the inputs INV1-INV2, respectively, of the error amplifiers 1-2.

The enable logic circuitry 1-2 is configured to receive the inputs ENBL1-ENBL2 and to provide outputs
5 PWRON1-PWRON2, respectively. With respect to the above-mentioned TPS51020 SMPC device, the inputs ENBL1-ENBL2 are TTL inputs. Further, in the event logical high level signals are provided at both of the inputs ENBL1-ENBL2, the oscillator 202 is turned-on; in the event logical low
10 level signals are provided at the inputs ENBL1-ENBL2, the oscillator 202 is turned-off.

In the presently disclosed embodiment, external capacitors C_{SS1}-C_{SS2} may be connected between the inputs SS/FS1-SS/FS2 and ground, respectively. For example,
15 suitable values of the capacitors C_{SS1}-C_{SS2} may be connected to the inputs SS/FS1-SS/FS2 for adjusting the soft-start time of the soft-start circuits 1-2. During normal operation of the soft-start circuits 1-2, constant currents generated by the current sources I_{S1}-I_{S2} flow
20 through the resistors R_{S1}-R_{S2} to charge the capacitors C_{SS1}-C_{SS2}, thereby ramping the voltage references VREF1A-VREF2A during start-up. It is noted that the capacitors C_{SS1}-C_{SS2} may be discharged by asserting FAULT1-FAULT2 high, respectively, or by asserting the inputs ENBL1-ENBL2 low.
25 Alternatively, parallel combinations of the external capacitors C_{SS1}-C_{SS2} and external resistors R_{SS1}-R_{SS2} may be connected between the inputs SS/FS1-SS/FS2 and ground, respectively.

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As described above, suitable values of the capacitors C_{SS1}-C_{SS2} are connected to the inputs SS/FS1-SS/FS2, respectively, to adjust the soft-start time of the soft-start circuits 1-2. Soft-start is achieved via

5   the soft-start circuits 1-2 by slowly ramping the error amplifier voltage references VREF1A-VREF2A by following a buffered version of the SS/FS1-SS/FS2 input voltages. It is noted that in an alternative embodiment, a desired start-up sequence may be obtained by providing suitable

10   external timing signals to the inputs SS/FS1-SS/FS2 since the start-up times do not depend on the load current. The soft-start time is programmable by the external capacitors C_{SS1}-C_{SS2} connected from the inputs SS/FS1-SS/FS2, respectively, to ground. Each of the inputs

15   SS/FS1-SS/FS2 sources a constant current, e.g., about 2.3 μA. The output voltage of the switch mode power converter ramps up from 0 volts to its target regulation voltage as the voltages on the inputs SS/FS1 and/or SS/FS2 increase from, e.g., 0 volts to about 1 volt.

20   Accordingly, a representative soft-start time formula may be expressed as

$$C_{SSx}(\text{Farads}) = T_{SS}(\text{sec}) \times 2.3 \times 10^{-6} \qquad (1)$$

25   As also described above, the oscillator output signal OSC_{OUT} has a frequency that is selected based on the states of the signals FREQSEL1-FREQSEL2. In the preferred embodiment,

$$\text{VREF1B} = \text{VREF2B} = 3.5 \text{ volts.} \qquad (2)$$

Accordingly, the state of the signals FREQSEL1-FREQSEL2 is logical high when only the capacitors C_{SS1}-C_{SS2} are connected between the inputs SS/FS1-SS/FS2 and ground, respectively. Further, the state of the signals FREQSEL1-FREQSEL2 is logical low when parallel combinations of the capacitors C_{SS1}-C_{SS2} and the resistors R_{SS1}-R_{SS2} are connected between the inputs SS/FS1-SS/FS2 and ground, respectively. Because the soft-start timing and the switching frequency selections are determined by the voltage levels at the inputs SS/FS1-SS/FS2, the selections of both the soft-start time and the switching frequency can be made at the same input pin of the converter.

In the presently disclosed embodiment, the oscillator control logic 204 is configured so that the frequency generated at the output OSC_{OUT} of the oscillator 102 is as described in the following TABLE:

TABLE

SS/FS1	SS/FS2	FREQUENCY (kHz)
C_{SS1} only to gnd	C_{SS2} only to gnd	High frequency
$R_{SS1}\|C_{SS1}$ to gnd	C_{SS2} only to gnd	Intermediate freq.
C_{SS1} only to gnd	$R_{SS2}\|C_{SS2}$ to gnd	Intermediate freq.
$R_{SS1}\|C_{SS1}$ to gnd	$R_{SS2}\|C_{SS2}$ to gnd	Low frequency

in which "C_{SSx} only to gnd" means that only the external capacitor C_{SSx} is connected between the designated input

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SS/FSx and ground, and "$R_{SSx} \| C_{SSx}$ to gnd" means that the parallel combination of R_{SSx} and C_{SSx} is connected between the designated input C_{SSx} and ground.

In the preferred embodiment,

$$R_{SS1} = R_{SS2} = 1 \text{ M}\Omega \qquad (3)$$
$$\text{High frequency} = 450 \text{ kHz} \qquad (4)$$
$$\text{Intermediate freq.} = 360 \text{ kHz} \qquad (5)$$
$$\text{Low frequency} = 270 \text{ kHz} \qquad (6)$$

Figs. 3a-3b depict illustrative soft-start voltage waveforms on the inputs SS/FS1-SS/FS2 and illustrative waveforms on the inputs ENBL1-ENBL2. Specifically, Fig. 3a depicts the soft-start voltage waveforms when the high frequency (e.g., 450 kHz) is the selected switching frequency, and Fig. 3b depicts the soft-start voltage waveforms when the intermediate frequency (e.g., 360 kHz) is the selected switching frequency.

As shown in Fig. 3a, the high switching frequency of 450 kHz is attained when both SS/FS1-SS/FS2 input voltages exceed 3.5 volts. The switching frequency begins with 270 kHz in a first stage of the soft-start from time t0 to time t1, increases to 360 kHz in a second stage of the soft-start from time t1 to time t2, and increases to 470 kHz at the steady state. As shown in Fig. 3b, the intermediate switching frequency of 360 kHz is attained when the SS/FS1 input voltage is kept below 3.5 volts and the SS/FS2 input voltage exceeds 3.5 volts. The switching frequency begins with 270 kHz in a first

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stage of the soft-start from time t0 to time t2, and increases to 360 kHz at the steady state. It is noted that when the low switching frequency of 270 kHz is the selected frequency, both of the SS/FS1-SS/FS2 input

5   voltages are kept below 3.5 volts so that the frequency is 270 kHz for the entire period of soft-start operation.

Accordingly, the switch mode power converter starts at a low frequency and switches over to higher frequencies, based on the SS/FS1-SS/FS2 input voltage

10   levels, only after the converter output voltage has stabilized. By linking the soft-start full scale range to the selection of higher order frequencies of the switch mode power converter, as depicted in Figs. 3a-3b, improved control of in-rush currents at start-up and

15   output voltage overshoots is achieved.

Having described the above illustrative embodiments, other alternative embodiments or variations may be made. For example, it was described that suitable values of the capacitors C_{SS1}-C_{SS2} and the resistors R_{SS1}-R_{SS2} may be

20   connected between the inputs SS/FS1-SS/FS2 and ground for determining the state at the inputs SS/FS1-SS/FS2 and for adjusting the soft-start time of the soft-start circuits 1-2. However, it should be understood that the advantages of the presently disclosed embodiment may be

25   achieved using any one-time use timing pin such as a soft-start timing pin (e.g., the SS/FS1-SS/FS2 input pins), a power-on reset timing pin, or any other suitable timing pin, so long as the ramp height of the timing signal exceeds its relevant dynamic range. For example,

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if a power-on reset ramp charges from 0-2 volts (*i.e.*, its relevant dynamic range is from 0-2 volts) and the supply voltage is equal to 5 volts, then the voltage range from 2-5 volts is unused. This unused portion of

5   the voltage range 0-5 volts may be employed for selectively clamping the timing ramp, thereby creating a decision point for a new mode of operation. In the presently disclosed embodiment, the resistors R_{SS1}-R_{SS2} are employed to clamp or not to clamp the soft-start signal,

10   thereby determining the state of the signals FREQSEL1-FREQSEL2 and the mode of operation of the oscillator. As described above, the oscillator is configured to generate multiple frequencies and is therefore capable of operating in a plurality of modes.

15   In addition, it should be understood that the resistors R_{SS1}-R_{SS2} were used to clamp the soft-start signal for purposes of illustration only. It should be appreciated that a diode or any other suitable element may be employed instead of or in conjunction with one or

20   more resistors to clamp the timing ramp.

It will be appreciated by those of ordinary skill in the art that modifications to and variations of the above-described frequency selection of switch mode power converters via soft-start voltage level may be made

25   without departing from the inventive concepts disclosed herein. Accordingly, the invention should not be viewed as limited except as by the scope and spirit of the appended claims.

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